MC10210

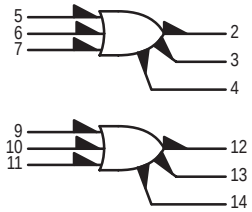
Dual 3-Input/3-Output OR Gate

The MC10210 is designed to drive up to six transmission lines simul– taneously. The multiple outputs of this device also allow the wire "OR"–ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10210 particularly useful in clock distribution applications where minimum clock skew is desired.

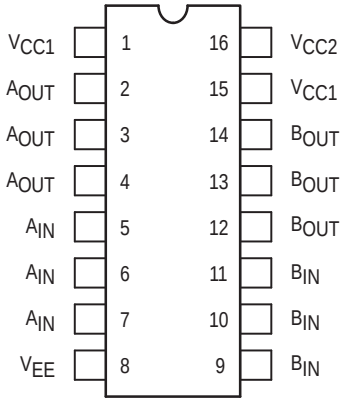
- P_D = 160 mW typ/pkg (No Loads)
- t_{pd} = 1.5 ns typ (All Output Loaded)
- t_r, t_f = 1.5 ns typ (20%–80%)

LOGIC DIAGRAM



V_{CC1} = PIN 1, 15
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP
PIN ASSIGNMENT

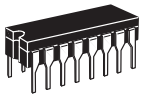


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

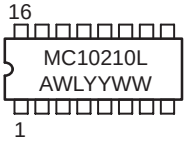
ON Semiconductor

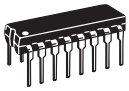
http://onsemi.com

MARKING DIAGRAMS

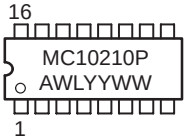


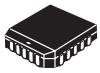
CDIP–16
L SUFFIX
CASE 620



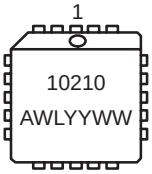


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10210L	CDIP–16	25 Units / Rail
MC10210P	PDIP–16	25 Units / Rail
MC10210FN	PLCC–20	46 Units / Rail

© Semiconductor Components Industries, LLC, 2000

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		42			38		42	mAdc
Input Current	I_{inH}	5, 6, 7		650			410		410	μAdc
	I_{inL}	5, 6, 7	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2 3 4	–1.060 –1.060 –1.060	–0.890 –0.890 –0.890	–0.960 –0.960 –0.960		–0.810 –0.810 –0.810	–0.890 –0.890 –0.890	–0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 4	–1.890 –1.890 –1.890	–1.675 –1.675 –1.675	–1.850 –1.850 –1.850		–1.650 –1.650 –1.650	–1.825 –1.825 –1.825	–1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 4	–1.080 –1.080 –1.080		–0.980 –0.980 –0.980			–0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 4		–1.655 –1.655 –1.655			–1.630 –1.630 –1.630		–1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{5+2+} t_{5-2-} t_{5+3+} t_{5-3-} t_{5+4+} t_{5-4-}	2 2 3 3 4 4	1.0 1.0 1.0 1.0 1.0 1.0	2.6 2.6 2.6 2.6 2.6 2.6	1.0 1.0 1.0 1.0 1.0 1.0	1.5 1.5 1.5 1.5 1.5 1.5	2.5 2.5 2.5 2.5 2.5 2.5	1.0 1.0 1.0 1.0 1.0 1.0	2.8 2.8 2.8 2.8 2.8 2.8	
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4	1.0 1.0 1.0	2.6 2.6 2.6	1.0 1.0 1.0	1.5 1.5 1.5	2.5 2.5 2.5	1.0 1.0 1.0	2.8 2.8 2.8	
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4	1.0 1.0 1.0	2.6 2.6 2.6	1.0 1.0 1.0	1.5 1.5 1.5	2.5 2.5 2.5	1.0 1.0 1.0	2.8 2.8 2.8	

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
	TEST VOLTAGE VALUES (Volts)				
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8					8	1, 15, 16
Input Current	I_{inH}	5, 6, 7	*				8	1, 15, 16
	I_{inL}	5, 6, 7		*			8	1, 15, 16
Output Voltage Logic 1	V_{OH}	2 3 4	5 6 7				8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Output Voltage Logic 0	V_{OL}	2 3 4					8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Threshold Voltage Logic 1	V_{OHA}	2 3 4			5 6 7		8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Threshold Voltage Logic 0	V_{OLA}	2 3 4				5 6 7	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Switching Times (50Ω Load)					**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{5+2+} t_{5-2-} t_{5+3+} t_{5-3-} t_{5+4+} t_{5-4-}	2 2 3 3 4 4			5 5 5 5 5 5	2 2 3 3 4 4	8 8 8 8 8 8	1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16 1, 15, 16
Rise Time (20 to 80%)	t_{2+} t_{3+} t_{4+}	2 3 4			5 5 5	2 3 4	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16
Fall Time (20 to 80%)	t_{2-} t_{3-} t_{4-}	2 3 4			5 5 5	2 3 4	8 8 8	1, 15, 16 1, 15, 16 1, 15, 16

* Individually test each input using the pin connections shown.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.